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BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1030

EXAMINER

BONURA, TIMOTHY M

ART UNIT	PAPER NUMBER
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2114

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/08/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No. 10/808,000	Applicant(s) BAARTMANS ET AL.	
	Examiner Tim Bonura	Art Unit 2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 20 December 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-32 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-5, 7-10 and 15-32 is/are rejected.
- 7) ☒ Claim(s) 6 and 11-14 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 24 March 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

- **Claim 11, 12 and 14 are objected under 37 CFR 1.75**
- **Claims 1-5, 7-10, and 15-32 are rejected under 35 U.S.C. 102(e) as being anticipated by Shinmori, et al, U.S. Patent Number 7,058,856**

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-5, 7-10, and 15-32 are rejected under 35 U.S.C. 102(e) as being anticipated by Shinmori, et al, U.S. Patent Number 7,058,856.

3. Regarding claim 1:

a. Regarding the limitation of "a logic structure integrated in an integrated circuit (IC), the logic structure having a set of bus inputs to generate events, a mask register to select inputs from among the set of bus inputs, a logic register to select logic to apply to the selected inputs and an event output to supply the result of the applied logic,"

Shinmori discloses a system with a semiconductor circuit with a memory device storing a program and data, a CPU to execute the process of the program and to store the data on the Flash ROM (Lines 10-15 of Column 2 also see Figure 5).

b. Regarding the limitation of "a bus interface integrated in the IC and coupled to the logic structure to transmit settable parameters to the mask register and the logic

register of the logic structure from an external agent," Shinmori discloses a system with control signals select the first input to the JTAG. (Lines 55-60 of Column 5).

4. Regarding claim 2, Shinmori discloses a system with a security bit that can be used to manage the data in the flash ROM for what data is received and selected for comparing. (Lines 65-67 of Column 5 and Lines 1-12 of Column 6).

5. Regarding claim 3, Shinmori discloses a system with a cmp register for comparing (Figure 5, item 27 and 24, Lines 38-46 of Column 5).

6. Regarding claim 4, Shinmori discloses a system with a TAP (test access port) coupled to a bus, the TAP used for testing and debugging of data through the CPU. (See Figure 5, item 14 with input bus from the left of the box, also Lines 60-65 of Column 5).

7. Regarding claim 5, Shinmori discloses a system with a sel logic to select data from the TAP or the CPU. (Figure 5, item 22, Lines 17-23 of Column 6).

8. Regarding claim 7, Shinmori discloses a system with a JTAG port for receive test data and a control circuit for controlling the received data. (Lines 50-65 of Column 5, see Figure 5, items 23, 12, and 11).

9. Regarding claim 8, Shinmori discloses a system with a JTAG port for communicating a TDO (test output data) to the external device for testing. (Lines 65-67 of Column 4 and Lines 1-2 of Column 5).

10. Regarding claim 9, Shinmori discloses a system with a security bit that can be used to manage the data in the flash ROM. (Lines 65-67 of Column 5 and Lines 1-12 of Column 6).

11. Regarding claim 10:

c. Regarding the limitation of "a counter register integrated in an integrated circuit and couple with an external unit integrated in the IC to receive results of operation from the external unit," Shinmori discloses a system with a security bit that can be used to

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manage the data in the flash ROM. (Lines 65-67 of Column 5 and Lines 1-12 of Column 6).

d. Regarding the limitation of "a logic structure integrated in the IC to receive signals from the external unit, to send operation to the external unit, to generate events based on the received external signals and received settable parameters, and to send the events to the counter register to after the operation of the counter register," Shinmori discloses a system with a semiconductor circuit with a memory device storing a program and data, a CPU to execute the process of the program and to store the data on the Flash ROM (Lines 10-15 of Column 2 also see Figure 5). Shinmori discloses a system with a TAP (test access port) coupled to a bus, the TAP used for testing and debugging of data through the CPU. (See Figure 5, item 14 with input bus from the left of the box, also Lines 60-65 of Column 5). External signals are received at eh JTAG port from a debugging device. (Lines 64-67 of Column 4).

e. Regarding the limitation of "a bus interface integrated in the IC and coupled to the logic structure to transmit settable parameters to the mask register and the logic register of the logic structure from an external agent," Shinmori discloses a system with control signals select the first input to the JTAG. (Lines 55-60 of Column 5).

12. Regarding claim 15, Shinmori discloses a system with a clock signal that is inputting through the JTAG port. (Figure 5, item 11, the TCK signal).

13. Regarding claim 16, Shinmori discloses a system with a security bit that can be used to manage the data in the flash ROM. (Lines 65-67 of Column 5 and Lines 1-12 of Column 6).

14. Regarding claim 17, Shinmori discloses a system with a security bit that can be used to manage the data in the flash ROM. (Lines 65-67 of Column 5 and Lines 1-12 of Column 6).

15. Regarding claim 18:

- f. Regarding the limitation of "receiving settable of parameters in a logic structure of an integrated circuit (IC)," Shinmori discloses a system a JTAG port for receiving parameters to be debugged. (See Figure 5, and Lines 64-67 of Column 4 and Lines 1-7 of Column 5).
 - g. Regarding the limitation of "receiving a set of bus inputs in the logic structure of the IC," Shinmori discloses a system a JTAG port for receiving data. (See Figure 5, and Lines 64-67 of Column 4 and Lines 1-7 of Column 5).
 - h. Regarding the limitation of "applying logic to the selected bus inputs in the logic structure to generate an event," Shinmori discloses a system with a TAP (test access port) coupled to a bus, the TAP used for testing and debugging of data through the CPU. (See Figure 5, item 14 with input bus from the left of the box, also Lines 60-65 of Column 5).
 - i. Regarding the limitation of "applying the events to a counter structure," Shinmori discloses a system with a security bit that can be used to manage the data in the flash ROM. (Lines 65-67 of Column 5 and Lines 1-12 of Column 6).
16. Regarding claim 19, Shinmori discloses a system with a JTAG port for communicating a TDO (test output data) to the external device for testing. (Lines 65-67 of Column 4 and Lines 1-2 of Column 5).
17. Regarding claim 20, Shinmori discloses a system with a security bit that can be used to manage the data in the flash ROM for what data is received and selected for comparing. (Lines 65-67 of Column 5 and Lines 1-12 of Column 6).
18. Regarding claim 21, Shinmori discloses a system with a security bit that can be used to manage the data in the flash ROM. (Lines 65-67 of Column 5 and Lines 1-12 of Column 6).

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19. Regarding claim 22, Shinmori discloses a system with a cmp register for comparing (Figure 5, item 27 and 24, Lines 38-46 of Column 5).

20. Regarding claim 23, Shinmori discloses a system with a sel logic to select data from the TAP or the CPU. (Figure 5, item 22, Lines 17-23 of Column 6).

21. Regarding claim 24:

j. Regarding the limitation of "receiving settable of parameters in a logic structure of an integrated circuit (IC)," Shinmori discloses a system a JTAG port for receiving parameters to be debugged. (See Figure 5, and Lines 64-67 of Column 4 and Lines 1-7 of Column 5).

k. Regarding the limitation of "receiving a set of bus inputs in the logic structure of the IC," Shinmori discloses a system a JTAG port for receiving data. (See Figure 5, and Lines 64-67 of Column 4 and Lines 1-7 of Column 5).

l. Regarding the limitation of "applying logic to the selected bus inputs in the logic structure to generate an event," Shinmori discloses a system with a TAP (test access port) coupled to a bus, the TAP used for testing and debugging of data through the CPU. (See Figure 5, item 14 with input bus from the left of the box, also Lines 60-65 of Column 5).

m. Regarding the limitation of "generating a system management interrupt based on the event," Shinmori discloses a system with a security bit that can be used to manage the data in the flash ROM. (Lines 65-67 of Column 5 and Lines 1-12 of Column 6).

22. Regarding claim 25, Shinmori discloses a system with a JTAG port for communicating a TDO (test output data) to the external device for testing. (Lines 65-67 of Column 4 and Lines 1-2 of Column 5).

23. Regarding claim 26, Shinmori discloses a system with a security bit that can be used to manage the data in the flash ROM for what data is received and selected for comparing. (Lines 65-67 of Column 5 and Lines 1-12 of Column 6).

24. Regarding claim 27, Shinmori discloses a system with a cmp register for comparing (Figure 5, item 27 and 24, Lines 38-46 of Column 5).

25. Regarding claim 28, Shinmori discloses a system with a sel logic to select data from the TAP or the CPU. (Figure 5, item 22, Lines 17-23 of Column 6).

26. Regarding claim 29:

n. Regarding the limitation of "receiving a set of bus inputs in a logic structure of an integrated circuit (IC)," Shinmori discloses a system a JTAG port for receiving parameters to be debugged. (See Figure 5, and Lines 64-67 of Column 4 and Lines 1-7 of Column 5).

o. Regarding the limitation of "applying a mask in the logic structure to select inputs from among the bus inputs," Shinmori discloses a system a JTAG port for receiving data. (See Figure 5, and Lines 64-67 of Column 4 and Lines 1-7 of Column 5). Shinmori discloses a system with a sel logic to select data from the TAP or the CPU. (Figure 5, item 22, Lines 17-23 of Column 6).

p. Regarding the limitation of "applying logic to the selected bus inputs in the logic structure to generate an event," Shinmori discloses a system with a TAP (test access port) coupled to a bus, the TAP used for testing and debugging of data through the CPU. (See Figure 5, item 14 with input bus from the left of the box, also Lines 60-65 of Column 5).

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- q. Regarding the limitation of “generating a system management interrupt based on the event,” Shinmori discloses a system with a security bit that can be used to manage the data in the flash ROM. (Lines 65-67 of Column 5 and Lines 1-12 of Column 6).
 - r. Regarding the limitation of “applying the events to a counter structure,” Shinmori discloses a system with a security bit that can be used to manage the data in the flash ROM. (Lines 65-67 of Column 5 and Lines 1-12 of Column 6).
 - s. Regarding the limitation of “providing the events over a bus to an external agent,” Shinmori discloses a system with a JTAG port for communicating a TDO (test output data) to the external device for testing. (Lines 65-67 of Column 4 and Lines 1-2 of Column 5).
27. Regarding claim 30, Shinmori discloses a system with a JTAG port for receive test data and a control circuit for controlling the received data. (Lines 50-65 of Column 5, see Figure 5, items 23, 12, and 11).
28. Regarding claim 31, Shinmori discloses a system with a security bit that can be used to manage the data in the flash ROM for what data is received and selected for comparing. (Lines 65-67 of Column 5 and Lines 1-12 of Column 6).
29. Regarding claim 32, Shinmori discloses a system with a cmp register for comparing (Figure 5, item 27 and 24, Lines 38-46 of Column 5).

Claim Objections

30. The numbering of claims is not in accordance with 37 CFR 1.126 which requires the original numbering of the claims to be preserved throughout the prosecution. When claims are canceled, the remaining claims must not be renumbered. When new claims are presented, they must be numbered consecutively beginning with the number next following the highest

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numbered claims previously presented (whether entered or not). Claims 11, 12, and 14 do not follow proper claim numbering. Please correct the numbering issues.

Allowable Subject Matter

31. Claims 6, 11-14 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

32. Applicant's arguments filed 12/20/2006 have been fully considered but they are not persuasive.

33. The examiner notes the argument concerning the claim objections of claims 11, 12, and 14. However, the applicant seems to not understand the point of the objections (see below for MPEP reference). The claim dependence of claims 11 and 12 is to claim 18. Claim 14 depends off of claim 11. Thereby, claims 11 and 12 depend from a claim that follows numerically the claims held in objection. Claim dependency can only come from preceding claims. (see MPEP 37 CFR 1.75 (page R-64 of MPEP) and MPEP 608.1(n) section II, last paragraph "Claims which are in improper dependent form for failing to further limit the subject matter of a previous claim should be objected to under 37 CFR 1.75(c)" emphasis add by examiner). If the applicant's representatives have any further questions regarding the claim objections, they are invited to call the examiner at the contact information listed below.

34. Regarding the arguments over claims 1-5, 7-10, 13, and 15-32, the examiner has fully considered the arguments but they are not persuasive.

35. Regarding claim 1:

t. The applicant argues that the rejections of the claims were not mapped to the out to the claim limitation. The examiner contends the prior art of record covers all the limitations in question. However, for clarity sake, the claims are mapped out as follows. (Please refer to Figure 5 for all references to the drawings). "A logic structure integrated into an IC" (all of Figure 5, Lines 39-40 of Column 1); "set of bus inputs to generate events" (items 11 and bus lines between 11 and 24, Lines 65-67 of Column 4 and Lines 1-8 of Column 5); "a mask register to select inputs" (Lines 57-59 of Column 5, the control signal which is not shown in figure 5, along with the SEL register item 22); "logic register to apply selected input" (Item 12 and 13, Column 5 Lines 55-56 the TAP and JTAG); "event output" (Lines 63-67 of Column 5 and Lines 1-5 of column 6, the output of the flash ROM).

u. The applicant further argues that the prior art does not teach the limitation of "a bus interface integrated in the IC and coupled to the logic structure to transmit settable parameters to the mask register and the logic register of the logic structure from an external agent." The examiner contends that the prior art does teach the limitation (see above rejection and response to argue (sub-paragraph "t"). The examiner contends the prior art does disclose a mask register and logic register that can send transmittable settings, applies the settings and outputs the results of the settings. (See rejection above).

36. Regarding claims 2-5, 7-10, 13 and 15-32, no other arguments are presented beyond the already discussed arguments concerning claim 1. Therefore, these claims rejections are maintained.

Conclusion

37. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

38. A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

39. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Tim Bonura**.

- The examiner can normally be reached on **Mon-Fri: 8:30-5:00**.
- The examiner can be reached at: **571-272-3654**.

40. If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisor, **Scott Baderman**.

- The supervisor can be reached on **571-272-3644**.

41. The fax phone numbers for the organization where this application or proceeding is assigned are:

- **703-872-9306 for all patent related correspondence by FAX.**

42. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

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applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov/>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

43. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the **receptionist** whose telephone number is: **571-272-2100**.

44. Responses should be mailed to:

- **Commissioner of Patents and Trademarks**

P.O. Box 1450

Alexandria, VA 22313-1450

tmb
March 4, 2007


SCOTT BADERMAN
SUPERVISORY PATENT EXAMINER